1. An apparatus within a processing system having multiple subsystems, for disassociating the power consumed by the processing system with instructions it is executing, the apparatus comprising:

a power prediction system, for providing a predictor of estimated power that will be consumed during execution of the instructions; and

a subsystem inhibition control, coupled to said power prediction system, for receiving said predictor, and for turning on/off selected ones of the subsystems based on the value of said predictor;

wherein by turning on/off ones of the selected subsystems, said subsystem inhibition control causes a total power consumption of the processing system to be disassociated with the instructions it is executing.

2. The apparatus as recited in claim 1 wherein said power prediction system comprises:

a power profile table having a plurality of power consumption entries, said entries corresponding to types of instructions that may be executed by the processing system.

3. The apparatus as recited in claim 2 wherein each of said power consumption entries comprises a plurality of power consumption values, said values corresponding to a predicted power consumption of an instruction within particular processing stages of the processing system.

4. The apparatus as recited in claim 1 wherein the multiple subsystems comprise:

a floating point unit; or

an media processing unit unit.

5. The apparatus as recited in claim 1 wherein said subsystem inhibition control comprises:

selection control, for determining which of the subsystems are available to be turned off; and

subsystem power profiles, coupled to said selection control, for specifying an estimated power consumption for each of the subsystems.

6. The apparatus as recited in claim 5 wherein said selection control utilizes said estimated power consumption for each of the subsystems to determine which, if any, of the subsystems to turn on/off.

7. The apparatus as recited in claim 5 wherein said selection control turns on/off ones of the subsystems via inhibit/burn signal lines.

8. The apparatus as recited in claim 1 wherein said subsystem inhibition control turns on/off selected ones of the subsystems to cause the total power consumption of the processing system to remain the same, regardless of which instructions are executing on the processing system.

9. The apparatus as recited in claim 1 wherein said subsystem inhibition control turns on/off selected ones of the subsystems to cause the total power consumption of the processing system to be random, regardless of which instructions are executing on the processing system.

10. The apparatus as recited in claim 1 further comprising:

a power counterweight, coupled to said power prediction system, to produce a counterweight current causing, in combination with said inhibition control, the total power consumption of the processing system to remain the same,

regardless of which instructions are executing on the processing system.

11. The apparatus as recited in claim 10 wherein said power counterweight is provided a maximum power threshold for the processing system, and configures said counterweight current such that the total power consumed by the processing system equals said maximum power threshold.

12. The apparatus as recited in claim 11 wherein said maximum power threshold is a default established during manufacture of the processing system.

13. The apparatus as recited in claim 11 wherein said maximum power threshold is configurable by software executing on the processing system.

14. A security system for a microprocessor based system having multiple subsystems for insuring that the power consumption of the microprocessor based system is not indicative of the instructions that it is executing, the security system comprising:

a power correlator, for estimating the power that the microprocessor based system will consume during execution of instructions; and

subsystem inhibition control, coupled to said power correlator, for utilizing said estimated power, and for selectively turning on/off ones of the multiple subsystems within the microprocessor based system during execution of the instructions;

wherein the ones of the multiple subsystems that are turned on/off are selected so as to disassociate the total power consumed by the microprocessor based system from the instructions it is executing.

15. The security system as recited in claim 14 wherein said subsystem inhibition control utilizes said estimated power to determine how much power must be

added to, or subtracted from said estimated power, to insure that the power consumption of the microprocessor based system is not indicative of the instructions it is executing.

16. The security system as recited in claim 15 wherein power is added to said estimated power by turning on said ones of the multiple subsystems.

17. The security system as recited in claim 15 wherein power is subtracted from said estimated power by turning off said ones of the multiple subsystems.

18. The security system as recited in claim 14 wherein said power correlator examines each instruction to be executed to estimate the power that said each instruction will consume as it executes.

19. The security system as recited in claim 18 wherein said power correlator estimates the power said each instruction will consume in each of a plurality of stages within a pipeline of the microprocessor based system.

20. The security system as recited in claim 14 wherein said power correlator comprises:

a power profile table having a plurality of power profile entries corresponding to a plurality of different instructions, said entries having a plurality of power estimates corresponding to power consumed in a plurality of different pipeline stages within the microprocessor based system.

21. The security system as recited in claim 20 wherein said power correlator further comprises:

a power profile register, coupled to said power profile table, for temporarily storing one of said power profile entries corresponding to one of said plurality of different instructions.

22. The security system as recited in claim 21 wherein said power profile register provides said one of said power profile entries to said power correlator.

23. The security system as recited in claim 14 wherein said subsystem inhibition control comprises:

subsystem power profiles, for indicating to inhibition control how much power each of the multiple subsystems consume when turned on.

24. An apparatus within a processing device having multiple subsystems for randomizing the total power consumed within the processing device, comprising:

a random value generator, for generating a random value as instructions are executed by the processing device; and

subsystem inhibition control, coupled to said random value generator, for turning on/off selected ones of the multiple subsystems;

wherein said subsystem inhibition control disassociates said instructions that are executed from power consumed by the processing device during their execution.

25. The apparatus as recited in claim 24 wherein said random value generator generates said random value between predetermined minimum and predetermined maximum values.

26. The apparatus as recited in claim 24 further comprising:

a total power predictor, coupled to said subsystem inhibition control, for providing an estimated

total power value to said subsystem inhibition control.

27. The apparatus as recited in claim 26 wherein said subsystem inhibition control utilizes said estimated total power value so that the total power consumed by the processing device does not exceed a predetermined threshold.

28. A computer program product for use with a computing device, the computer program product comprising:

a computer usable medium, having computer readable program code embodied in said medium, for causing a processing device having multiple subsystems to be described, said computer readable program code comprising:

first program code for providing a power prediction system for providing a predictor of estimated power that will be consumed during execution of instructions by the processing device; and

second program code for providing a subsystem inhibition control, coupled to said power prediction system, for receiving said

predictor, and for turning on/off selected ones of the subsystems based on the value of said predictor.

29. The computer program product, as recited in claim 28 wherein by turning on/off ones of the selected subsystems, said subsystem inhibition control causes a total power consumption of the processing device to be disassociated with the instructions it is executing.

30. The computer program product, as recited in claim 28 further comprising:

third program code for providing a power profile table having a plurality of power consumption entries, said entries corresponding to types of instructions that may be executed by the processing device.

31. The computer program product as recited in claim 28 wherein said subsystem inhibition control comprises:

selection control, for determining which of the subsystems are available to be turned off; and

subsystem power profiles, coupled to said selection control, for specifying an estimated power consumption for each of the subsystems.

32. The computer program product as recited in claim 31 wherein said selection control utilizes said estimated power consumption for each of the subsystems to determine which, if any, of the subsystems to turn on/off.

33. The computer program product as recited in claim 28 wherein said subsystem inhibition control turns on/off selected ones of the subsystems to cause the total power consumption of the processing device to remain the same, regardless of which instructions are executing on the processing device.

34. The computer program product as recited in claim 28 wherein said subsystem inhibition control turns on/off selected ones of the subsystems to cause the total power consumption of the processing device to be random, regardless of which instructions are executing on the processing device.

35. A method for disassociating the power that is consumed by a microprocessor having multiple subsystems, from the instructions that it is executing, the method comprising:

estimating the power that will be consumed by each instruction in the microprocessor; and

selectively turning on/off ones of the multiple subsystems such that the total power consumed by the microprocessor is unrelated to the instructions that are executing.

36. The method as recited in claim 35 wherein said step of turning on/off ones of the multiple subsystems causes the total power consumed by the microprocessor to be invariant.

37. The method as recited in claim 35 wherein said step of turning on/off ones of the multiple subsystems causes the total power consumed by the microprocessor to be random.

38. A computer data signal embodied in a transmission medium comprising:

computer-readable first program code for providing a power correlator that estimates the power that will be consumed as an instruction executes on a microprocessor having multiple subsystems; and

computer-readable second program code for providing subsystem inhibition control, for utilizing the estimated power, and for selectively turning on/off ones of the multiple subsystems within the microprocessor during execution of the instructions.

39. The computer data signal of claim 38 wherein the ones of the multiple subsystems that are turned on/off are selected so as to disassociate the total power consumed by the microprocessor from the instructions it is executing.

40. The computer data signal of claim 38 wherein said subsystem inhibition control utilizes said estimated power to determine how much power must be added to, or subtracted from said estimated power, to insure that

the power consumption of the microprocessor is not indicative of the instructions it is executing.